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APPROVAL

CUSTOMER:

PART NUMBER:	**CT49248NS246D2**
DESCRIPTION:	**Combo Memory (Green MCP)** **NAND Flash 1Gb (x8) + DDR3 SDRAM 1Gb (x16)** **Outline:10.5x13.5x1.2mm, Pitch:0.8mm, FBGA 128Balls**
CUSTOMER'S P/N:	
CHECKED BY:	
APPROVED BY:	
DATE:	
Remark	

Approved Signatures	鉅景科技 股份有限公司
	Contact Person:

1. INTRODUCTION

CT49248NS246D2 is a Multi Chip Package Memory (MCP) that integrated 1G bits NAND Flash and 1G bits DDR3 SDRAM by advanced SiP (System-in-a-Package) technology. CT49248NS246D2 offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

1.1 Application

- DSC
- DV
- PMP

1.2 Feature

PRODUCT LIST

- CT49248NS246D2
  - NAND FLASH: 1G bits (128M x 8-bit)
  - DDR3 SDRAM: 1G bits (8M x 8-Bank x 16-bit)

POWER SUPPLY

- NAND FLASH
  - 3.3V
- DDR3 SDRAM
  - 1.5V

PACKAGE

- FBGA 10.5 x 13.5 x 1.2 mm, 128 Balls
- Pin Pitch: 0.8 mm
- Weight: TBD

Temperature

- Operating: -10 to +85 °C
- Storage: -55 to +125 °C

NAND FLASH

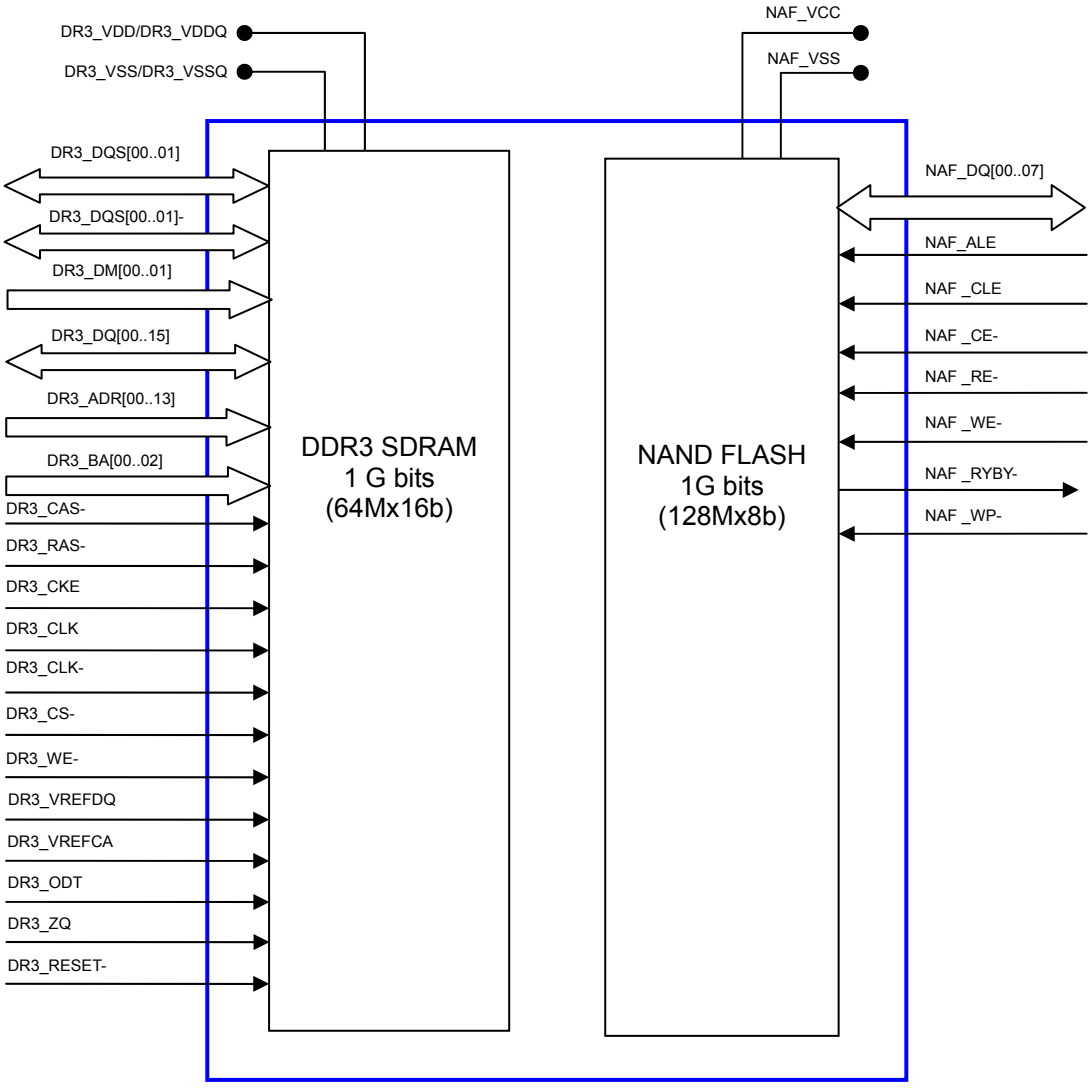
- Voltage Supply
  - 3.3V Device: 2.7V ~ 3.6V
- Organization
  - Memory Cell Array: (128M + 4M) x 8bit
  - Data Register: (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program: (2K + 64)Byte
  - Block Erase: (128K + 4K)Byte
- Page Read Operation
  - Page Size: (2K + 64)Byte
  - Random Read: 25μs(Max.)
  - Serial Access: 30ns(Min.)
- Fast Write Cycle Time
  - Page Program time: 200μs(Typ.)
  - Block Erase Time: 2.0ms(Typ.)
- Command/Address/Data Multiplexed NAF_DQ[00..07] Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance: 100K Program/Erase Cycles(with 1bit/528Byte ECC)
  - Data Retention: 10 years
- Command Driven Operation

DDR3 SDRAM

- DR3_VDD, DR3_VDDQ = 1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (DR3_CLK, DR3_CLK-)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- POSTED CAS ADDITIVE latency (AL)
- Programmable CAS WRITE latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- TC of -10°C to +95°C
  - 64ms, 8192 cycle refresh at -10°C to +85°C
  - 32ms, 8192 cycle refresh at +85°C to +95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

2. FUNCTION DIAGRAM

2.1 MCP



3. PIN CONFIGURATION

3.1 CT49248NS246D2 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11
A	NAF_WP-	DR3_VDDQ	DR3_DQ13	DR3_DQ15				DR3_DQ12	DR3_VDDQ	DR3_VSS	NAF_RYBY-
B	NAF_WE-	DR3_VSSQ	DR3_VDD	DR3_VSS				DR3_DQS01-	DR3_DQ14	DR3_VSSQ	NAF_RE-
C	NAF_ALE	DR3_VDDQ	DR3_DQ11	DR3_DQ09				DR3_DQS01	DR3_DQ10	DR3_VDDQ	NAF_CE-
D	NAF_CLE	DR3_VSSQ	DR3_VDDQ	DR3_DM01				DR3_DQ08	DR3_VSSQ	DR3_VDD	NAF_VCC
E	NAF_VSS	DR3_VSS	DR3_VSSQ	DR3_DQ00				DR3_DM00	DR3_VSSQ	DR3_VDDQ	NC
F	NC	DR3_VDDQ	DR3_DQ02	DR3_DQS00				DR3_DQ01	DR3_DQ03	DR3_VSSQ	NC
G	NC	DR3_VSSQ	DR3_DQ06	DR3_DQS00-				DR3_VDD	DR3_VSS	DR3_VSSQ	NC
H	NC	DR3_VREFDQ	DR3_VDDQ	DR3_DQ04				DR3_DQ07	DR3_DQ05	DR3_VDDQ	NC
J	NC	NC	DR3_VSS	DR3_RAS-				DR3_CLK	DR3_VSS	NC	NC
K	NAF_VSS	DR3_ODT	DR3_VDD	DR3_CAS-				DR3_CLK-	DR3_VDD	DR3_CKE	NAF_VCC
L	NC	NC	DR3_CS-	DR3_WE-				DR3_ADR10 /AP	DR3_ZQ	NC	NC
M	NC	DR3_VSS	DR3_BA0	DR3_BA2				NC	DR3_VREFCA	DR3_VSS	NC
N	NAF_DQ03	DR3_VDD	DR3_ADR03	DR3_ADR00				DR3_ADR12 /BC-	DR3_BA1	DR3_VDD	NAF_DQ04
P	NAF_DQ02	DR3_VSS	DR3_ADR05	DR3_ADR02				DR3_ADR01	DR3_ADR04	DR3_VSS	NAF_DQ05
R	NAF_DQ01	DR3_VDD	DR3_ADR07	DR3_ADR09				DR3_ADR11	DR3_ADR06	DR3_VDD	NAF_DQ06
T	NAF_DQ00	DR3_VSS	DR3_RESET-	DR3_ADR13				NC	DR3_ADR08	DR3_VSS	NAF_DQ07

TOP VIEW

6. PACKAGE DIMENSION (128 Balls FBGA, 10.5x13.5x1.2mm)