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Brief Datasheet

PRODUCT: **CT84966D1**

DESCRIPTION: **Combo Memory (Green MCP)**
DDR3 SDRAM 4Gb (x16)
Outline:10.5x13.5x1.2mm, Pitch:0.8mm, TFBGA 128 Balls

Approved Signatures	鉅景科技 股份有限公司
	Contact Person:

1. INTRODUCTION

CT84966D1 is a Multi Chip Package Memory (MCP) that integrated 2G bits x2 DDR3 SDRAM by advanced SiP (System-in-a-Package) technology. CT84966D1 offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

1.1 APPLICATION

- DSC
- DV
- PMP
- DSLR
- Entertainment

1.2 FEATURES

PRODUCT LIST

- CT84966D1
  - DDR3 SDRAM: 4G bits (32M x 8-Bank x 16-bit)

POWER SUPPLY

- DDR3 SDRAM
  - 1.5V

PACKAGE

- TFBGA 10.5 x 13.5 x 1.2 mm, 128 Balls
- Ball Pitch: 0.8 mm
- Weight: TBD

Temperature

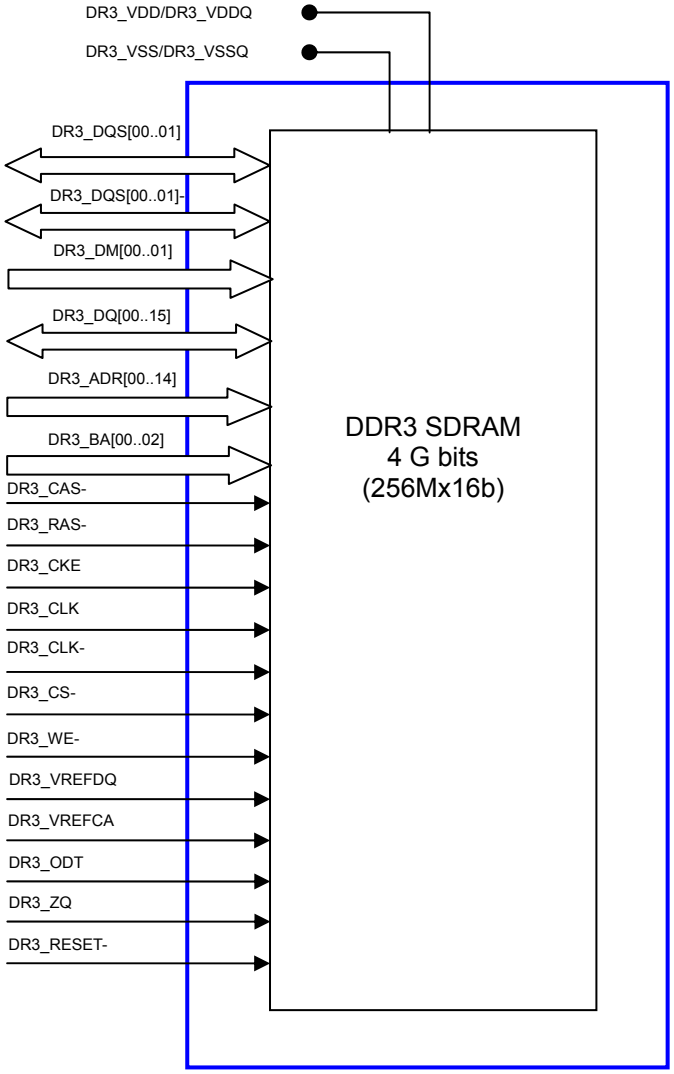
- Operating: -10 to +85 °C
- Storage: -55 to +125 °C

DDR3 SDRAM

- DR3_VDD = DR3_VDDQ = +1.5V ±0.075V
- 1.5V center-terminated push/pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (DR3_CLK, DR3_CLK-)
- 8 internal banks
- Nominal and dynamic on-die termination (DR3_ODT) for data, strobe, and mask signals
- Programmable DR3_CAS- READ latency (CL)
- POSTED CAS ADDITIVE latency (AL)
- Programmable CAS WRITE latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- TC of 0°C to +95°C
  - 64ms, 8192 cycle refresh at 0°C to +85°C
  - 32ms, 8192 cycle refresh at +85°C to +95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

2. FUNCTION DIAGRAM

2.1 MCP



3. PIN CONFIGURATION

3.1 PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11
A	NC	DR3_VDDQ	DR3_DQ13	DR3_DQ15				DR3_DQ12	DR3_VDDQ	DR3_VSS	NC
B	NC	DR3_VSSQ	DR3_VDD	DR3_VSS				DR3_DQS01-	DR3_DQ14	DR3_VSSQ	NC
C	NC	DR3_VDDQ	DR3_DQ11	DR3_DQ09				DR3_DQS01	DR3_DQ10	DR3_VDDQ	NC
D	NC	DR3_VSSQ	DR3_VDDQ	DR3_DM01				DR3_DQ08	DR3_VSSQ	DR3_VDD	NC
E	NC	DR3_VSS	DR3_VSSQ	DR3_DQ00				DR3_DM00	DR3_VSSQ	DR3_VDDQ	NC
F	NC	DR3_VDDQ	DR3_DQ02	DR3_DQS00				DR3_DQ01	DR3_DQ03	DR3_VSSQ	NC
G	NC	DR3_VSSQ	DR3_DQ06	DR3_DQS00-				DR3_VDD	DR3_VSS	DR3_VSSQ	NC
H	NC	DR3_VREFDQ	DR3_VDDQ	DR3_DQ04				DR3_DQ07	DR3_DQ05	DR3_VDDQ	NC
J	NC	NC	DR3_VSS	DR3_RAS-				DR3_CLK	DR3_VSS	NC	NC
K	NC	DR3_ODT	DR3_VDD	DR3_CAS-				DR3_CLK-	DR3_VDD	DR3_CKE	NC
L	NC	NC	DR3_CS-	DR3_WE-				DR3_ADR10/AP	DR3_ZQ	NC	NC
M	NC	DR3_VSS	DR3_BA0	DR3_BA2				NC	DR3_VREFCA	DR3_VSS	NC
N	NC	DR3_VDD	DR3_ADR03	DR3_ADR00				DR3_ADR12/BC-	DR3_BA1	DR3_VDD	NC
P	NC	DR3_VSS	DR3_ADR05	DR3_ADR02				DR3_ADR01	DR3_ADR04	DR3_VSS	NC
R	NC	DR3_VDD	DR3_ADR07	DR3_ADR09				DR3_ADR11	DR3_ADR06	DR3_VDD	NC
T	NC	DR3_VSS	DR3_RESET-	DR3_ADR13				DR3_ADR14	DR3_ADR08	DR3_VSS	NC

4. PACKAGE DIMENSION (128 Balls TFBGA, 10.5x13.5x1.2mm)