

## 1. INTRODUCTION

CT92246B1 is a Multi Chip Package Memory (MCP) that integrated 1G bits Mobile DDR SDRAM by advanced SiP (System-in-a-Package) technology. CT92246B1 offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

### 1.1 Application

- Feature Phone
- Smart Phone
- MID

### 1.2 Features

#### PRODUCT LIST

- CT92246B1
  - Mobile DDR SDRAM: 1G bits (16M x4-Bank x16-bit)

#### POWER SUPPLY

- MOBILE DDR SDRAM
  - 1.7-1.9V

#### PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- TFBGA 8x10x1.2 mm, 60 Balls
- Ball Pitch: 0.8 mm
- Weight: TBD

#### Temperature

- Operating: 0 to +85 °C
- Storage: 0 to +150°C

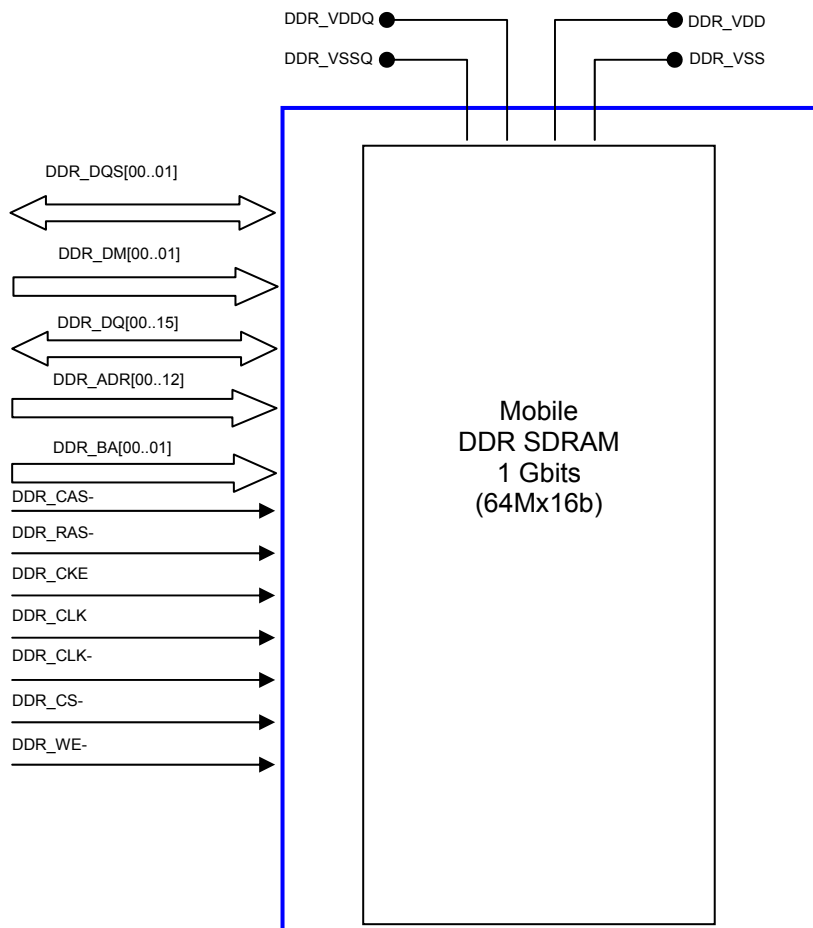
#### Mobile DDR SDRAM

- 4 banks x 16M x 16 organization
- Data Mask for Write Control (DDR\_DM[00..01])
- Four Banks controlled by DDR\_BA00 & DDR\_BA01
- Programmable DDR\_CAS- Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  - 2, 4, 8 for Sequential Type
  - 2, 4, 8 for Interleave Type
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 cycles/64ms
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DDR\_DQS[00..01]) for input and output data, active on both edges
- Differential clock inputs DDR\_CLK and DDR\_CLK-
- Drive Strength (DS) Option: Full, 1/2, 1/4, 1/8

- Auto Temperature-Compensated Self Refresh (Auto TCSR)
- Partial-Array Self Refresh (PASR) Option: Full, 1/2, 1/4, 1/8, 1/16
- Deep Power Down (DPD) mode

## 2. FUNCTION DIAGRAM

### 2.1 MCP



### 3. PIN CONFIGURATION

#### 3.1 Pin Assignment

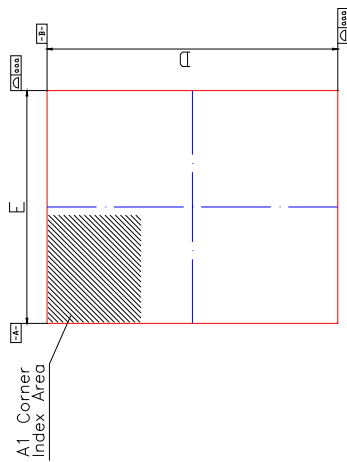
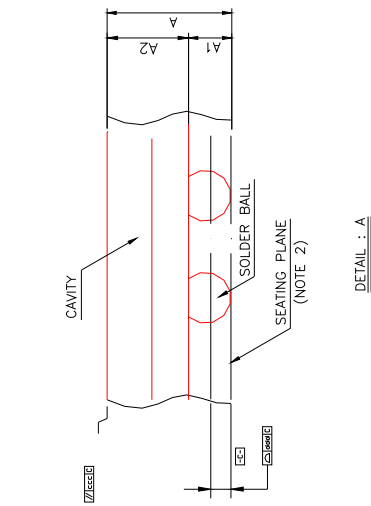
	01	02	03	04	05	06	07	08	09
<b>A</b>	DDR_VSS	DDR_DQ15	DDR_VSSQ				DDR_VDDQ	DDR_DQ00	DDR_VDD
<b>B</b>	DDR_VDDQ	DDR_DQ13	DDR_DQ14				DDR_DQ01	DDR_DQ02	DDR_VSSQ
<b>C</b>	DDR_VSSQ	DDR_DQ11	DDR_DQ12				DDR_DQ03	DDR_DQ04	DDR_VDDQ
<b>D</b>	DDR_VDDQ	DDR_DQ09	DDR_DQ10				DDR_DQ05	DDR_DQ06	DDR_VSSQ
<b>E</b>	DDR_VSSQ	DDR_DQS01	DDR_DQ08				DDR_DQ07	DDR_DQS00	DDR_VDDQ
<b>F</b>	DDR_VSS	DDR_DM01	NC				NC	DDR_DM00	DDR_VDD
<b>G</b>	DDR_CKE	DDR_CLK	DDR_CLK-				DDR_WE-	DDR_CAS-	DDR_RAS-
<b>H</b>	DDR_ADR09	DDR_ADR11	DDR_ADR12				DDR_CS-	DDR_BA00	DDR_BA01
<b>J</b>	DDR_ADR06	DDR_ADR07	DDR_ADR08				DDR_ADR10	DDR_ADR00	DDR_ADR01
<b>K</b>	DDR_VSS	DDR_ADR04	DDR_ADR05				DDR_ADR02	DDR_ADR03	DDR_VDD

TOP VIEW

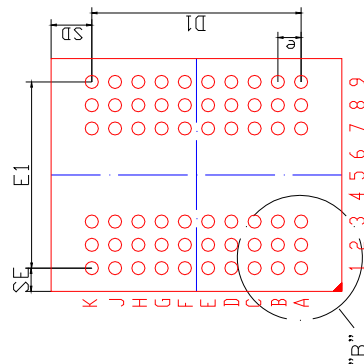
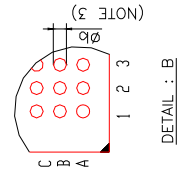
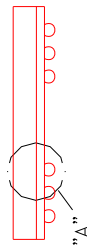
5. PACKAGE DIMENSION (60 Ball VFBGA, 8x10x1.2mm)

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.25
A1	0.32	0.36	0.40
A2	---	---	0.85
D	9.90	10.00	10.10
E	7.90	8.00	8.10
D1	---	7.2	---
E1	---	6.4	---
SE	---	0.8	---
SD	---	1.4	---
e	---	0.8	---
b	0.40	0.45	0.50
aaa	---	0.15	---
ccc	---	0.20	---
ddd	---	0.12	---
MD/ME	---	9/10	---

- NOTE :
1. CONTROLLING DIMENSION : mm.
  2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
  3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
  4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .



TOP VIEW



BOTTOM VIEW

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